What is claimed

1. An Active Pixel CMOS image sensor device including at least one pixel circuit, comprising:

at least one transistor of a first conductivity type; and

at least one transistor of a second conductivity type, said transistor of the second conductivity type being used for resetting the body of the transistor of the first conductivity type.

2. The Active Pixel CMOS image sensor according to Claim 1, wherein at least one pixel is sensing photo-generated charge by means of modulation of transistor threshold using transistor threshold body effect.

3. The device according to Claim 1, wherein at least one p-type and one n-type transistor share a common gate bus line.

4. The device according to Claim 1, wherein a separate bus line is provided to at least one pixel to supply a reset voltage, and wherein the reset voltage may be changed depending on the pixel.

5. The device according to Claim 4, including an array of pixels in a column, and wherein the reset voltage is changed depending on

pixel address within a column of pixels of the array to compensate for the pixel threshold differences along the said column of pixels.

6. The device according to Claim 3, wherein the common gate bus line consists of a stack of at least two conductor layers separated by a dielectric layer, the first layer of the stack being connected to pixel transistor gates, and said conductor layers of the stack being connected to respective driving circuits at the periphery of the pixel array.

7. An Active Pixel CMOS image sensor device including at least one pixel circuit, comprising:

an array of an MxN arrangement of pixels, where the M is at least 1 and N is at least 1;

a column signal bus line for each column in the array, each column connected to clamping transistors for clamping the bus line potential to a reference voltage when the pixels of the array are not addressed.

8. The image sensor of Claim 7 where column sense and reset buses are connected to column signal processing circuit modules, and where circuit modules are sensing column signals when a row of pixels is addressed.

9. The image sensor according to claim 8, wherein the circuit modules have the capability to store the column signals after sensing in a digital form, and in an analog form on capacitors after a strobe command is applied to the modules.

10. The image sensor according to Claim 7, wherein column sense and reset buses are connected to column switches that supply a pixel signal to column holding capacitors, and a pixel reset error voltage, one by one, in a serial fashion to an external processing circuit block.

11. The image sensor according to Claim 10, wherein said circuit block has the capability to compute a reset voltage correction bias based on the supplied reset error signal and feed it back, one by one, in a serial fashion to appropriate column reset bus lines to cause a zero signal pixel output to equal a given reference voltage, thereby canceling the pixel offset.

12. The image sensor according to Claim 10, wherein the circuit block for computing the reset bias to eliminate the pixel offset error is a DSP.

13. The image sensor according to Claim 8, wherein said circuit modules have the capability to supply bias to the pixel reset buses after an error command is applied to the modules, said bias being adjusted in a manner as to cause the zero signal pixel output to equal a given reference voltage.

14. The image sensor according to Claim 10, wherein a pixel offset error voltage is detected and stored in pixels by means of applying at least two consecutive readout and reset pulses to the pixels of the array, and wherein the first readout and reset pulse sequence is used for the photo-signal detection and the second readout and reset pulse sequence is used for the offset detection and compensating offset correction storage.

15. The image sensor according to Claim 7, including address (row) line drivers, address (row) line decoders, address (row) line shift registers, column shift registers, column decoders, column amplifiers, column scanner switches, output signal amplifiers, and other CMOS logic circuits included on the same substrate with the pixel array.